

PRELIMINARY AMENDMENT

Serial Number: Unknown

Filing Date: Herewith

Title: STRUCTURE AND METHOD FOR DUAL GATE OXIDE THICKNESSES

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56. (New) The structure of claim 55, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).
57. (New) The structure of claim 55, wherein first dielectric layer of a first thickness includes silicon dioxide (SiO_2) and the top layer includes silicon nitride (Si_3N_4).
58. (New) The structure of claim 55, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).
59. (New) The structure of claim 55, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.
60. (New) The structure of claim 55, wherein the top layer includes a top layer of silicon nitride (Si_3N_4) which comprises approximately a third of the first thickness of the first dielectric layer.
61. (New) The structure of claim 55, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.
62. (New) A logic device and a memory device structure on a single substrate, comprising:
a first transistor, wherein the first transistor includes:
a first dielectric layer of a first thickness less than 5 nanometers (nm);
a top layer which exhibits a high resistance to boron penetration at high temperatures; and
a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness.
63. (New) The structure of claim 62, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

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64. (New) The structure of claim 62, wherein first dielectric layer of a first thickness includes silicon dioxide (SiO_2) and the top layer includes silicon nitride (Si_3N_4).
65. (New) The structure of claim 62, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).
66. (New) The structure of claim 62, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.
67. (New) A logic device and a memory device structure on a single substrate, comprising:
a first transistor, wherein the first transistor includes:
a first dielectric layer of a first thickness less than 5 nanometers (nm);
a silicon nitride (Si_3N_4) top layer which exhibits a high resistance to oxidation at high temperatures; and
a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness.
68. (New) The structure of claim 67, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).
69. (New) The structure of claim 67, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).
70. (New) The structure of claim 67, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.
71. (New) The structure of claim 67, wherein the silicon nitride (Si_3N_4) top layer includes a silicon nitride (Si_3N_4) top layer with a thickness of approximately a third of the first thickness of the first dielectric layer.

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72. (New) The structure of claim 67, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.
73. (New) A logic device and a memory device structure on a single substrate, comprising:
a first transistor, wherein the first transistor includes:
a first dielectric layer of a first thickness less than 5 nanometers (nm);
a top layer of approximately a third of the first thickness, which exhibits a high resistance oxidation at high temperatures; and
a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness.
74. (New) The structure of claim 73, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.
75. (New) The structure of claim 73, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).
76. (New) The structure of claim 73, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO₂).
77. (New) The structure of claim 73, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.
78. (New) A logic device and a memory device structure on a single substrate, comprising:
a first transistor, wherein the first transistor includes:
a first dielectric layer of a first thickness less than 5 nanometers (nm);
a top layer which exhibits a high resistance to oxidation at high temperatures; and
a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness of less than 12 nanometers (nm).

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79. (New) The structure of claim 78, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.
80. (New) The structure of claim 78, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).
81. (New) The structure of claim 78, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).
82. (New) A logic device and a memory device structure on a single substrate, comprising:
a first transistor, wherein the first transistor includes:
 a first dielectric layer of a first thickness less than 5 nanometers (nm);
 a silicon nitride (Si_3N_4) top layer of approximately a third of the first thickness,
which exhibits a high resistance to oxidation at high temperatures; and
 a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness of less than 12 nanometers (nm).
83. (New) The structure of claim 82, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.
84. (New) The structure of claim 82, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).
85. (New) The structure of claim 82, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

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86. (New) A logic device and a memory device structure on a single substrate formed by the method comprising:
- forming a pair of transistor channel regions on the single substrate;
 - forming a pair of gate oxides to a first thickness on the pair of channel regions;
 - wherein forming the pair of gate oxides to a first thickness includes forming the pair of gate oxides to a thickness of less than 5 nanometers (nm) by krypton plasma generated atomic oxygen at approximately 400 degrees Celsius;
 - forming a thin dielectric layer on one of the pair of gate oxides, wherein the thin dielectric layer exhibits resistance to oxidation at high temperatures; and
 - forming the other of the pair of gate oxides to a second thickness.